31. (Twice Amended) A memory cell, comprising:

a [lateral] transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the first plate;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first plate of the first source/drain region, the first plate including a surface layer of polysilicon that is etch- roughened , and an insulator layer that separates the second polysilicon plate from the etch-roughened polysilicon surface of the first plate .

33. (Amended) A memory cell, comprising:

a [lateral] transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the first plate;

wherein the trench capacitor includes a second plate of polysilicon formed in the trench so as to surround the first plate , and an insulator layer that separates the second polysilicon plate from at least the etch-roughened surface of the first plate.

36. (Twice Amended) The memory device of claim 35, wherein the access transistor [comprises a lateral transistor] <u>includes a body region of p-type single crystalline silicon adjoining the first source/drain region, wherein the first source/drain region is n-type single crystalline silicon</u>.

41. (Twice Amended) A memory cell, comprising:

a [lateral] transistor comprising outwardly from a substrate a first source/drain region at least a portion of which serves as a single crystalline first capacitor plate for forming a conductorless connection of the transistor to a trench capacitor, a body region and a second source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the lateral transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor; and

an insulator layer that separates the second polycrystalline semiconductor plate from the micro-roughened surface of the first plate.

**Please add the following new claim:**

51. (New) A memory cell comprising:

a lateral transistor formed in an upper portion of a single crystalline substrate and including a first source/drain region, a body region, and a second source/drain region;

a trench capacitor including a first plate formed by the substrate;

a trench formed in the substrate, the trench including a micro-roughened polysilicon surface, a second plate formed within the trench, and a dielectric layer separating the micro-roughed polysilicon trench surface from the second plate; and

a contact connecting the second source/drain region to the second plate.

## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 10, 2001, and the references cited therewith.

Claims 17, 31, 33, 36 and 41 are amended, and claim 51 is added; as a result, claims 17-51 are now pending in this application.